Amendment to the Claims:

1. (Currently Amended) A method of stabilizing two current loops within a circuit comprising the steps of:

providing a main current loop utilizing negative feedback for supplying current to a load;

providing a sensing loop utilizing negative feedback for controlling the current to the load but not supplying current thereto;

an error amplifier for the main current loop coupled to the output of an error amplifier for the sensing loop such that the capacitance of each loop is isolated from that of the other loop; and

providing a compensating capacitor to each loop whereby stability is independently maintained for each loop within selected operational criteria.

2. (Currently Amended) A method according to claim 1 wherein the coupling step further comprises coupling the output of the error amplifier for the sensing loop to the gate of a transistor and coupling the compensating capacitor of the sensing loop to the source of the transistor.

3. (Previously Presented) A method according to claim 1 wherein the output of the main loop error amplifier comprises a first node having a higher impedance than a second node, the compensating capacitor being coupled to the second node.

4. (Previously Presented) A method according to claim 1 wherein the output of the main loop error amplifier comprises a first node having a higher impedance than a second node, the compensating capacitor being coupled to the first node.

5. (Original) A circuit stabilization method according to claim 1 wherein the main loop further comprises a low dropout regulator (LDO).

6. (Currently Amended) A circuit having a low capacitive load and comprising two stable current loop sub circuits further comprising:

a main current loop for supplying current to the load, the main current loop having a negative feed back loop utilizing a first compensation capacitor for maintaining stability within a pre-selected operational range;

a sensing loop for controlling the current to the load but not supplying current thereto, the sensing loop having a negative feedback loop utilizing a second compensation capacitor for maintaining stability within a pre-selected operational range; and

a transistor for coupling the output of the main current loop error amplifier and the output of the sensing loop such that the first compensation capacitor is isolated from the second compensation capacitor.

7. (Original) A circuit according to claim 6 wherein the transistor further comprises a MOSFET.

8. (Original) A circuit according to claim 6 wherein the transistor further comprises a bipolar transistor.

9. (Previously Presented) A circuit having a low capacitive load and comprising two stable current loop sub circuits further comprising:

a main current loop for supplying current to the load, the main current loop having a first compensation capacitor for maintaining stability within a pre-selected operational range;

a sensing loop for controlling the current to the load, the sensing loop having a second compensation capacitor for maintaining stability within a pre-selected operational range; and

a transistor for coupling the output of the main current loop error amplifier and the output of the sensing loop such that the first compensation capacitor is isolated from the second compensation capacitor, wherein the output of the main current loop error amplifier is coupled to the gate of the transistor and the output of the sensing loop error amplifier is coupled to the source of the transistor via the second compensation capacitor.

10. (Previously Presented) A circuit according to claim 6 wherein the main loop further comprises a main load error amplifier having a plurality of output nodes and wherein the output of the main loop error amplifier comprises a lower impedance node of the error amplifier.

11. (Previously Presented) A circuit according to claim 6 wherein the main loop error amplifier further comprises an error amplifier having a plurality of output nodes and wherein the output of the main loop comprises a higher impedance node of the error amplifier.

12. (Original) A circuit according to claim 6 wherein the main loop further comprises a low dropout regulator (LDO).

13. (Original) A circuit according to claim 6 wherein the load capacitance of the circuit is on the order of approximately 1uF.

14. (Currently Amended) A method of stabilization of a circuit having a capacitive load on the order of approximately 1uF and having two current loop sub circuits comprising

the steps of:

providing a main current loop for supplying current to the load, the main current loop utilizing negative feedback and having a first compensation capacitance for maintaining stability within a pre-selected operational range;

providing a sensing loop for limiting maximum current to the load but not supplying current thereto, the sensing loop utilizing negative feedback and having a second compensation capacitance for maintaining stability within a pre-selected operational range; and

coupling the output of the main current loop error amplifier and the output of the sensing loop error amplifier such that the first compensation capacitance is isolated from the second compensation capacitance.

15. (Previously Presented) A method of stabilization of a circuit having a capacitive load on the order of approximately 1uF and having two current loop sub circuits comprising the steps of:

providing a main current loop for supplying current to the load, the main current loop having a first compensation capacitance for maintaining stability within a pre-selected operational range;

providing a sensing loop for limiting maximum current to the load, the sensing loop having a second compensation capacitance for maintaining stability within a pre-selected operational range; and

coupling the output of the main current loop error amplifier and the output of the sensing loop error amplifier such that the first compensation capacitance is isolated from the second compensation capacitance, wherein the output of the main current loop is coupled to the gate of a transistor and one terminal of the sensing loop compensation capacitor is coupled to the source of the transistor.

16. (Previously Presented) The method according to claim 14 wherein the output of the main loop further comprises an error amplifier having a plurality of output nodes and wherein the output of the main loop comprises a lower impedance node of the error amplifier.

17. (Previously Presented) The method according to claim 14 wherein the main loop further comprises an error amplifier having a plurality of output nodes and wherein the output of the main loop error amplifier comprises a higher impedance node of the error amplifier.

18. (Original) The method according to claim 14 used in a low dropout regulator (LDO).

19. (Previously Presented) The method of Claim 1 wherein the sensing loop limits the maximum current to the load.

20. (Previously Presented) The circuit of Claim 6 wherein the sensing loop limits the maximum current to the load.